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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/810,746	03/16/2001	Ohad Falik	P04931 (NATI15-04931)	6880

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EXAMINER	
MASON, DONNA K	
ART UNIT	PAPER NUMBER
2111	3

DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/810,746	FALIK ET AL.	
	Examiner	Art Unit	
	Donna K. Mason	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-69* is/are pending in the application.

4a) Of the above claim(s) *7-49 and 61-69* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 50-60* is/are rejected.

7)☒ Claim(s) *52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-6 and 50-60, drawn to a system and method for allowing shared access by at least two processors including an embedded controller and a host processor to at least two modules, classified in class 710, subclass 240.

   II. Claims 7-17 and 61-63, drawn to a system for allowing shared access and a method for preventing shared access by at least two processors including an embedded controller and a host processor to at least one module, the system including a main power supply, classified in class 713, subclass 300.

   III. Claims 18-31, 47-49, and 64-68, drawn to a system and method for allowing shared access by at least two processors including an embedded controller and a host processor to at least one module, and a system for increasing throughput to at least one module, classified in class 710, subclass 240.

   IV. Claims 32-46, drawn to a system for allowing concurrent access to at least one module by at least two processors including an embedded controller and a host processor, classified in class 710, subclass 240.

V. Claim 69, drawn to a system for allowing shared access by at least two processors including an embedded controller and a host processor to one or more modules, the system operable to allow concurrent access, and including a main power supply, an alternative power supply, and an embedded controller bus interface, classified in class 710, subclass 240.

2. The inventions are distinct, each from the other because of the following reasons:

3. Inventions I, II, III, IV, and V are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)).

4. In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the combination (Invention V) as claimed does not set forth the details of the subcombinations (Inventions I, II, III, and IV) as claimed. In the combination, the subcombinations are broadly recited, and the specific characteristics set forth in the subcombination claims are not set forth in the combination claim. Because claims to both the subcombinations and combination are presented and assumed to be patentable, the omission of details of the claimed subcombinations in the combination claim is evidence that the patentability of the combination does not rely on the details of the specific subcombinations.

5. The subcombination of Invention I has separate utility such as in systems and methods that include a bus extension.

6. The subcombination of Invention II has separate utility such as in systems and methods that include a domain separator.

7. The subcombination of Invention III has separate utility such as in systems and methods that include an error indication.

8. The subcombination of Invention IV has separate utility such as in systems and methods that include an index register.

9. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Groups II, III, IV, or V, restriction for examination purposes as indicated is proper.

10. In response to the Restriction Requirement mailed December 16, 2003 (*see* Paper No. 7, filed January 26, 2004), a provisional election was made with traverse to prosecute the invention of Group I, claims 1-6 and 50-60. Affirmation of this election must be made by applicant in replying to this Office Action. Claims 7-49 and 61-69 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

11. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Specification

12. The disclosure is objected to because of the following informalities:

On page 30, line 13, "typical module 241" is recited. However, in Fig. 10, items 241 are both described as "functional modules". It is recommended that applicant review the specification and the drawings, making corrections where necessary, to provide consistency in the description for item 241.

Appropriate correction is required. See 37 CFR 1.71.

Claim Objections

13. Claim 52 is objected to because of the following informalities:

In line 2, insert --.-- after "access".

Appropriate correction is required. See 37 CFR 1.75.

Claim Rejections - 35 USC § 112

14. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

15. Claim 53 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

16. Claim 53 recites a method for allowing an embedded controller to access "at least two modules affiliated with a device," including the steps of "indicating the device" and "indicating one of the at least two modules for accessing". It appears that the steps

of "indicating the device" and "indicating one of the at least two modules for accessing", are redundant in view of the limitation regarding the at least two modules being affiliate with a device. For examination purposes, claim 52 has been interpreted such that the step of "indicating the device" is the same as the step of "indicating one of the at least two modules for accessing."

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

18. Claims 1-6 and 50-60 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,260,098 to Ku.

With regard to independent claim 1, Ku discloses a system (Fig. 5, item 600) for allowing shared access by at least two processors including an embedded controller (Fig. 5, item 620 and column 11, lines 19-21) and a host processor (Fig. 5, item 602) to at least two modules (Fig. 5, items 622 and 622b) including: at least two modules (Fig. 5, items 622 and 622b); and a transaction control (Fig. 5, item 100); wherein the embedded controller is capable of providing an indication of which of the at least two

modules to access to said transaction control (column 5, lines 34-61); and the host processor is capable of providing an indication of which of the at least two modules to access to said transaction control (column 5, lines 2-33 and lines 54-61).

With regard to independent claim 50, Ku discloses a method for allowing shared access to at least two modules (Fig. 5, items 622 and 622b) by at least two processors including an embedded controller (Fig. 5, item 620 and column 11, lines 19-21) and a host processor (Fig. 5, item 602), including the steps of: receiving an indication from each of the at least two processors of a module from among the at least two modules to access (column 5, lines 9-53); arbitrating between the at least two processors in favor of one of the at least two processors (column 5, lines 2-8); and accessing said module indicated by said one of the at least two processors (column 5, lines 30-33 and column 6, lines 18-20).

With regard to dependent claims 2, 3, 51 and 52, Ku discloses the method and system, the method further including the step of: blocking access by another of the at least two processors to said module indicated by said one of the at least two processors (column 4, lines 57-63), and where the indication from each of the at least two processors is for a different module to access (column 5, lines 54-67 to column 6, lines 1-17).

With regard to claim 4, Ku discloses the system, further including: a bus extension (Fig. 5, item 112), where at least one of the at least two modules is accessible via said bus extension (Fig. 5, item 622 and 622b); and where the transaction control is capable of providing to said bus extension an indication of said at least one of the

modules, accessible via said bus extension, for access by the host processor; said transaction control is capable of providing to said bus extension an indication of said at least one of the modules, accessible via said bus extension, for access by the embedded controller; and said bus extension is capable of providing an indication of said at least one of the modules for access by one of the processors (column 5, lines 2-61).

With regard to claims 5 and 6, Ku discloses the system, where the transaction control is capable of providing an indication of at least one of the at least two modules for access by one of the processors (column 5, lines 2-61), and where at least one of the at least two modules is part of an input/output chip (column 7, lines 20-59).

With regard to claim 53, Ku discloses a method for allowing an embedded controller (Fig. 5, item 620) to access at least two modules (Fig. 5, items 622 and 622b and Fig. 6, item 622) affiliated with a device, including the steps of: indicating the device (column 5, lines 54-61); indicating an access direction (read/write) (column 8, lines 61-65); indicating one of the at least two modules for accessing (column 5, lines 54-61); indicating a location for accessing, within said indicated one of the at least two modules (Fig. 6, item 622 and column 7, lines 20-59); and transferring data between said indicated location and the embedded controller (column 7, lines 41-50).

With regard to claims 54-55, Ku discloses the method where the indicated one of the at least two modules is accessible via a bus extension (Fig. 5, item 112), and where the step of indicating one of the at least two modules for accessing includes the step of:

indicating one of at least one chip select corresponding to said bus extension for accessing (column 5, lines 2-61).

With regard to claims 56-60, Ku discloses the method where indicated one of the at least two modules is part of an input/output chip (column 7, lines 20-59), and where the step of indicating a location for accessing includes the step of providing an indication of a location for accessing via an internal bus to said indicated one of said at least two modules, the method further including the step of: waiting for the freeing up of said internal bus before transferring said indication of a location for accessing onto said internal bus (column 5, lines 2-61).

Therefore, Ku reads on the invention as claimed.

19. Claims 1-6 and 50-60 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication No. 2002/0129184 to Watanabe.

With regard to claim 1-3 and 5, Watanabe discloses a system (Fig. 1, item 100) for allowing shared access by at least two processors (Fig. 1, items 110 and 160) including an embedded controller (Figs. 1, 2A, and 2B, item 160) and a host processor (Figs. 1, 2A, and 2B, item 110) to at least two modules including (paragraph [0017]): at least two modules (Fig. 1, items 170 and 180); and a transaction control (Fig. 1, item 150); wherein the embedded controller is capable of providing an indication of which of the at least two modules to access to said transaction control; and the host processor is capable of providing an indication of which of the at least two modules to access to said transaction control (paragraph [0017]).

With regard to claims 4 and 6, Watanabe discloses the system, further including: a bus extension (Fig. 1, item 165), wherein at least one of the at least two modules is accessible via said bus extension; and wherein said transaction control is capable of providing to said bus extension an indication of said at least one of the modules, accessible via said bus extension, for access by the host processor; said transaction control is capable of providing to said bus extension an indication of said at least one of the modules, accessible via said bus extension, for access by the embedded controller; and said bus extension is capable of providing an indication of said at least one of the modules for access by one of the processors, and the system where at least one of the at least two modules is part of an input/output chip (paragraph [0015]).

With regard to claims 50-52, Watanabe discloses a method for allowing shared access to at least two modules by at least two processors including an embedded controller and a host processor (Figs. 1, 2A, and 2B), including the steps of: receiving an indication from each of the at least two processors of a module from among the at least two modules to access; arbitrating between the at least two processors in favor of one of the at least two processors; and accessing said module indicated by said one of the at least two processors (paragraphs [0017] and [0018]).

With regard to claim 53, Watanabe discloses a method for allowing an embedded controller to access at least two modules affiliated with a device (Fig. 2A), including the steps of: indicating the device (paragraphs [0017] and [0018]); indicating an access direction (read/write) (paragraph [0015]); indicating one of the at least two modules for accessing (paragraphs [0017] and [0018]); indicating a location for accessing, within

said indicated one of the at least two modules; and transferring data between said indicated location and the embedded controller (paragraphs [0017] and [0018]).

With regard to claims 54 and 55, Watanabe discloses the method where the indicated one of the at least two modules is accessible via a bus extension, and where the step of indicating one of the at least two modules for accessing includes the step of: indicating one of at least one chip select corresponding to said bus extension for accessing (Fig. 2A, item 170).

With regard to claims 56-60, Watanabe discloses the method where the indicated one of the at least two modules is part of an input/output chip (paragraph [0015]), where the step of indicating a location for accessing includes the step of providing an indication of a location for accessing via an internal bus to said indicated one of said at least two modules, the method further including the step of: waiting for the freeing up of said internal bus before transferring said indication of a location for accessing onto said internal bus (paragraphs [0018] and [0019]).

Therefore, Watanabe reads on the invention as claimed.

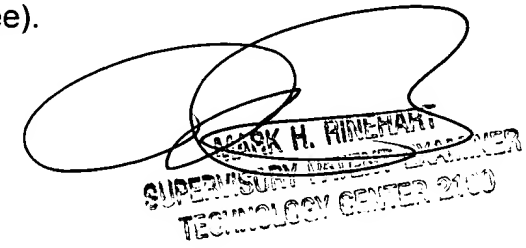
Conclusion

20. A shortened statutory period for reply is set to expire THREE MONTHS from the mailing date of this communication. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this communication.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (703) 305-1887. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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